What is claimed is :

1. An integrated circuit (IC) structure utilized in a standard cell, comprising:

a substrate including pluralities of circuit elements; and

m metal layers, which are disposed on said substrate and utilized as connection layout for circuit elements, wherein each metal layer further including an isolation layer for electrical isolation among metal layers;

said structure is characterized in that one terminal of at least one circuit element is arranged with a circuit passageway, said circuit passageway extends from said substrate to n metal layers such that any connection line in each metal layer can be connected with said terminal by said circuit passageway, wherein n is larger than 1 and n is less than m+1.

2. The IC structure of claim 1, wherein each circuit passageway connects through two metal layers.

3. The IC structure of claim 1, wherein each circuit passageway connects through three metal layers.

4. The IC structure of claim 1, wherein said circuit passageway can be formed by pluralities of metal layers and pluralities of vias.

5. The IC structure of claim 1, wherein said standard cell can be assembled as an intellectual property element.

6. The IC structure of claim 1, wherein said standard cell can be assembled as an intellectual property element library.

7. An integrated circuit (IC) layout design method utilized for connection of elements in a standard cell, wherein said IC comprises a substrate, said substrate further including pluralities of circuit elements; and m metal layers disposed on said substrate, which are utilized as connection layout for circuit elements, wherein each metal layer further including an isolation layer for electrical isolation among metal layers; said IC layout

design method comprising the following steps:

arranging a circuit passageway at one terminal of a circuit element, said circuit passageway extends from said substrate through at least two metal layers; and

connecting a line, which is required to be electrically connected to said terminal, to said terminal by connecting said line to said circuit passageway.

8. The IC layout design method of claim 7, wherein said circuit passageway connects through two metal layers.

9. The IC layout design method of claim 7, wherein said circuit passageway connects through three metal layers.

10. The IC layout design method of claim 7, wherein said standard cell can be connected to an intellectual property element.

11. The IC layout design method of claim 7, wherein said standard cell can be connected to an intellectual property element library.